



# 1 SOFT TRANSITION CONVERTER

## 2 Background of Invention

### 3 1. *Field of the Invention*

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7 This invention relates to DC-to-DC converters, DC-to-AC inverters and AC-to-DC converters. The major  
8 characteristic of this power conversion technique is that primary switching elements switches at zero voltage and  
9 the secondary rectifiers means have negligible reverse recovery losses.

### 10 2. *Description of the Prior Art*

11 There is a continuing industry demand for increasing power density, which means more power transferred in a  
12 given volume. A method for increasing the power transfer through the converter is to increase the switching  
13 frequency in order to minimize the size of magnetic and the capacitors. Using prior art topologies such as forward  
14 or flyback, which employ "hard" switching techniques makes high frequency operation less efficient. The  
15 switching losses associated with switching elements, which turn on when there is a voltage across them, are  
16 proportional with the switching frequency. An increase in switching frequency leads to an increase in switching  
17 losses and an increase in level of electromagnetic interference (EMI).  
18

19 In order to overcome limitations in switching speeds, the prior art has devised a new family of soft transition.  
20 The patent # 5,132,889 , # 5,126,931 , # 5,231,563 , # 5,434,768 present several methods of accomplishing  
21 zero voltage switching across the primary switches.  
22 Another power loss mechanism is due to the reverse recovery in the output rectifiers. During switching when a  
23 negative polarity voltage is applied to a rectifier in conduction the current through the rectifier will continue to  
24 conduct until all the carriers in the rectifier's junctions are depleted. During this period of time the current  
25 polarity will reverse, the current flowing ~~form~~ <sup>from</sup> the cathode to the anode, while the voltage across the diode is still  
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1 positive from the anode to the cathode. The current flowing in reverse through the diode will reach a peak value  
2 referred in literature as  $I_{rrm}$ . Further on, while the rectifiers' junction is depleting the carriers, the rectifier  
3 becomes a high impedance device. The current through the rectifier will decrease rapidly from  $I_{rrm}$  level to zero.  
4 During the same time the negative voltage across the rectifier will build up to high levels.

5 During the period of time when there is a negative voltage across the diode and negative current is flowing  
6 through it, there will be power dissipation in the device. This kind of loss is referred in the literature as reverse  
7 recovery losses. The reverse recovery loss is proportional with the reverse recovery current  $I_{rrm}$ , the negative  
8 voltage across the rectifier and the frequency.

9 The reverse recovery current  $I_{rrm}$ , which is a key component in reverse recovery loss, is function of <sup>a</sup> ~~the~~ type of <sup>this</sup>  
device, the temperature and the current slope at turn off. The reverse recovery characteristics are getting <sup>a</sup> ~~worst~~  
10 higher voltage rectifiers. As a result the reverse recovery loss becomes a significant loss mechanism for higher  
11 output voltage applications. The reverse recovery current  $I_{rrm}$  is direct dependent of the current slope at turn off.  
A soft slope reduces the reverse recovery current and as a consequence reduces the reverse recovery loss. To  
13 accomplish a very soft slope current at turn off an inductive element has to be in series with the rectifier. The  
14 inductor element will prevent a fast current variation  $dI/dt$ . The presence of an inductive element in series with the  
15 rectifier will increase the negative voltage across the rectifier at turn off. The reverse voltage across the rectifier  
16 can reach very high levels and can exceed the voltage break down of the device, leading to failure.

17 RC snubbers or complicated lossless snubers can be added across the rectifier to reduce the reverse recovery loss  
18 and the voltage stress on the devices. This leads to complex circuits and which negatively affects the efficiency  
19 and the reliability. As a result of these limitations the high voltage converters have to operate at lower frequency  
20 in order to reduce the power dissipation associated with reverse recovery.

21 What is needed is a converter topology which can operate at constant frequency with zero voltage switching on  
22 the primary switches and soft commutation on the output rectifiers, wherein low current slope through the  
23 rectifiers at turn off is associated with low negative voltage across the rectifiers. The lowest voltage across the  
24 output rectifiers in a DC-DC converter is the output voltage. As a result our goal is to reduce the negative voltage  
25 across the output rectifier to the level of the output voltage.

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2      **Brief Summary of the Invention**

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4      The invention applies to topologies in which the voltage in the secondary of the transformer has three states.

5      One state wherein the voltage in the secondary is a positive voltage source, another stage wherein the voltage in

6      the secondary of the transformer is zero with a very low internal impedance and the third stage wherein the

7      voltage in the secondary of the transformer is a negative voltage source. To provide such secondary signal we

8      have identified three topological structures. One is the full bridge phase shifted topology. The second topology is a

9      half bridge utilizing and additional bydirectional switch, depicted in Figure 9A. The third topology is two

10     transistors forward phase shifted, depicted in Figure 14A.

11     All these topologies operate in a similar manner. An input voltage source is applied to the primary of a

12     transformer through controlled switching elements. The primary winding of the transformer has two terminations.

a      For simplicity we are going to refer to ~~one~~<sup>one</sup> end of the primary winding of the transformer as a dotted end. The

13     secondary winding of the transformer has also two terminations. When a voltage is applied to the primary winding

14     of the transformer with the positive polarity at the dotted end, a voltage will be induced in the secondary. The

15     termination of the secondary winding where the voltage induced has a positive polarity is referred as a dotted end

16     of the secondary winding.

17     The input voltage source is applied to the primary winding of the transformer through two controlled switching

18     elements. A control-switching element is an electronic switch, which can be controlled by a control signal to

19     exhibit low impedance when the switching element is turned ON or large impedance when the switching element

20     is turned OFF. The input voltage source is applied to the primary winding through two controlled switching

21     devices, which connects the termination of the transformer to the termination of the input voltage source

22     selectively. The dotted end of the primary winding of the transformer can be connected to the positive end of the

23     input voltage source and the other end of the primary winding of the transformer is connected to the negative end

24     of the input voltage source. This operation will be further referred to as positive voltage across the primary

25     winding.

1 The controlled switching elements can connect *also* the dotted end of the primary winding of the transformer to  
2 the negative end of the input voltage source and the other end of the primary winding of the transformer is  
3 connected to the positive end of the input voltage source. This operation will be further referred as negative  
4 voltage across the primary winding.

5 The control switching elements can also short out the primary winding of the transformer by applying low  
6 ~~impedance~~ impedance across the winding. This operation will be further referring to as the dead time.

7 The controlled switching elements can be controlled in a such way to apply sequentially a positive voltage across  
8 the primary winding for given period of time, referred as positive ON time, short the primary winding for a period  
9 of time, referred as dead time, apply a negative voltage across the primary winding for a given period of time,  
10 referred as negative ON time, equal as duration with the positive ON time. If the summation of positive ON time,  
11 dead time and negative ON time is constant, the mode of operation is referred as constant frequency operation.

12 The power converter can also operate in frequency modulation mode, wherein the summation of positive ON time,  
13 dead time and negative ON time is not constant. We introduce the term of duty cycle, which is defined as the ratio  
14 between the summation of positive and negative ON time and the summation of the positive ON time, twice the  
15 dead time and negative ON time. By varying the duty cycle the power transferred through the transformer can be  
16 controlled. The duty cycle can be varied by varying the duration of the positive and negative ON time, for the  
17 constant frequency operation. For variable frequency operation the duty cycle control can be made by maintaining  
18 the negative and positive ON time constant and varying the dead time, or by varying the positive and negative ON  
19 time and maintain the dead time constant or by varying the positive and negative ON time and the dead time in the  
20 same time. Important is to have the positive ON time equal to the negative ON time. Another important element of  
21 this technology is the low bydirectional impedance across the secondary winding of the transformer, wherein the  
22 secondary current can flow freely in both directions.

23 One key element in this invention is an additional inductor element in series with the secondary winding, labeled  
24 soft commutation inductor. The inductor can be also located in the primary section in series with the primary  
25 winding of the transformer. The soft commutation inductive element can be also split, one section located in the  
26 primary , in series with the primary winding and an another section in the secondary in series with the secondary  
27 winding. In the case when the soft commutation inductor is located in the secondary, there is a bydirectional

1 rectification means connected in series with it and the secondary winding. A bridge of rectifiers can form the  
2 bydirectional rectification means. Across the capacitor element is connected the load. The bridge of rectifiers has a  
3 first input terminal, a second input terminal, a first output terminal and a second output terminal. The first rectifier  
4 is connected between the first input terminal and the first output terminal with the cathode to the first output  
5 terminal, the second rectifier is connected between the second input terminal and the first output terminal, with the  
6 cathode to the first output terminal. The third rectifier is connected between the second input terminal and the  
7 second output terminal with the cathode to the second input terminal, the fourth rectifier is connected between the  
8 first input terminal and the second output terminal with the cathode to the first input terminal. The AC voltage  
9 source in series with said inductive element is connected between the first input terminal and the second input  
10 terminal. The output capacitor is in parallel with the load is connected between the first output terminal and the  
11 second output terminal.

12 The bydirectional rectification means can be <sup>also</sup> constructed using two rectifiers and two capacitors.

13 The bridge of rectifiers means and capacitors having a first input terminal a second input terminal a first output  
14 terminal and a second output terminal. The first rectifier is connected between the first input terminal and the first  
15 output terminal with the cathode to the first output terminal, the second rectifier is connected between the first  
16 input terminal and the second output terminal, with the cathode to the first input terminal. The first capacitor is  
17 connected in between the first output terminal and the second input terminal, and the second capacitor is  
18 connected between the second input terminal and the second output terminal. The said AC voltage source is in  
19 series with the soft commutation inductive element and connected between the first input terminal and the second  
20 input terminal. The load is connected between the first output terminal to the second output terminal.

21 During the positive and negative ON time the power is transferred from the primary to the secondary via the  
22 transformer, the soft commutation inductor, and the bydirectional rectifier means to the load. In the same time  
23 energy is stored in the soft commutation inductor. During the dead time, the energy stored in the soft commutation  
24 inductor is further transferred to the load. There are two modes of operation. One mode of operation referred as  
25 discontinuous conduction mode, the entire energy stored in the soft commutation inductor is transferred to the  
26 load prior the change of the voltage polarity on the transformer. The second mode of operation referred as  
27 continuous mode, there is still energy left in the soft commutation inductor prior the reversal of the voltage

1 polarity in the transformer. The discontinuous mode of operation has the advantage of transferring the energy  
2 from the primary to the secondary unidirectional at each cycle. The continuous mode of operation will transfer the  
3 energy left in the soft commutation diode back to the primary before the next energy transfer from primary to the  
4 secondary starts.

5 A critical conduction mode of operation can be implemented wherein the reversal of the voltage polarity in the  
6 transformer is accomplished just after the entire energy in the soft commutation inductor is transferred to the  
7 secondary. This leads to a modulation in frequency, wherein the frequency will increase at light loads, and  
8 decrease at heavy loads. A mix mode of operation can be also implemented wherein some high frequency  
9 boundary or low frequency boundaries or both are set. There are several major advantages of this topology.

10 One of the major advantages is the fact that the voltage across the rectifiers is clamped to the output voltage. There  
11 is not ringing or spike across the rectifiers which exceed the output voltage. The voltage across the rectifiers for a  
12 given output voltage is the lowest theoretical possible. In most of the topologies operating over a range of input  
13 and output voltages the voltage across the rectifiers can be several times larger than the output voltage. For a single  
14 ended forward converter the output voltage is  $V_r = (V_{in_{Max}}/V_{in_{Min}}) * V_o / D_{Max}$ , wherein  $V_{in_{Max}}$  &  $V_{in_{Min}}$  is the  
15 maximum and minimum input voltage and  $D_{Max}$  is the maximum duty cycle, and  $V_o$  is the output voltage. For an  
16 input voltage range of 2:1 and 50% maximum duty cycle, the reverse voltage across the rectifier is  $4 * V_o$ . In  
17 conclusion in these topologies we achieve the lowest voltage across the rectifiers for a given output voltage.

18 Another major advantage of this topology is the fact that the current slope through the rectifier at turn off is  
19 controlled by the soft commutation inductor. As a result there is a controlled  $dI/dt$ . A soft current through the  
20 rectifier at turn OFF reduces considerably the reverse recovery current. The clamped voltage across the output  
21 rectifiers in association with the soft current slope at turn OFF leads to reduced reverse recovery losses. If the  
22 circuits operate in continuous mode the reverse recovery losses are reduced, and if we operate in discontinuous  
23 conduction mode the reverse recovery losses are actually eliminated. This is due to the fact that the current through  
24 the rectifiers reaches zero prior the reverse voltage is applied to them.

25 The invention can be better visualized by turning to the following drawings.

1      **Brief Description of the Drawings**

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3      **Figure 1** is a schematic of a converter utilizing the power transfer methodology of the invention.

4      **Figure 1B** is a timing diagram of the circuit of Figure 1.

5      **Figure 2** is a schematic diagram of an AC-DC converter wherein prior art technique is illustrated.

6      **Figure 3A** is a schematic diagram of a DC-DC Converter wherein another prior art technique is illustrated.

7      **Figure 3B** is a timing diagram of the circuit of Figure 3A.

8      **Figure 4A** is a schematic diagram of an AC-DC Converter using an embodiment of this invention.

9      **Figure 4B** is a timing diagram of the circuit of Figure 4A.

10     **Figure 5A** is a schematic diagram of an AC-DC Converter using another embodiment of this invention.

11     **Figure 5B** is a timing diagram of the circuit of Figure 5A.

12     **Figure 6A** is a schematic diagram of an AC-DC Converter using an embodiment of this invention depicted in  
13     Figure 4A, operating in continuous mode.

14     **Figure 5B** is a timing diagram of the circuit of Figure 6A.

15     **Figure 7A** is a schematic diagram of an AC-DC Converter using another embodiment of this invention.

16     **Figure 7B** is a timing diagram of the circuit of figure 7A.

17     **Figure 8A** is a schematic diagram of a DC-AC Converter, utilizing a phase shift bridge topology suitable with the  
18     AC-DC converters depicted in several embodiments of the invention.

19     **Figure 8B** is a timing diagram of the circuit of figure 8A.

20     **Figure 9A** is a schematic diagram of an DC-AC Converter, utilizing a half bridge topology employing an  
21     additional bydirectional switch, topology suitable with the AC-DC converters depicted in several embodiments of  
22     the invention.

23     **Figure 9B** is a timing diagram of the circuit of figure 9A.

24     **Figure 10A** is a schematic diagram of an AC-DC Converter depicted in Figure 4A wherein two of the rectifiers  
25     are replaced by synchronous rectifiers.

26     **Figure 10B** is a timing diagram of the circuit of figure 10A.

1      **Figure 11A** is a schematic diagram of an AC-DC Converter depicted in Figure 4A wherein all of the rectifiers are  
2      replaced by synchronous rectifiers.  
3      **Figure 11B** is a timing diagram of the circuit of figure 11A.  
4      **Figure 12A** is a schematic diagram of an AC-DC Converter depicted in Figure 5A wherein all of the rectifiers are  
5      replaced by synchronous rectifiers.  
6      **Figure 12B** is a timing diagram of the circuit of figure 12A.  
7      **Figure 13A** is a schematic diagram of an DC-DC Converter using the embodiment presented in Figure 4A,  
8      wherein the soft commutation inductor is transferred in primary section in series with the primary winding. The  
9      AC signal across the primary winding connected in series with the soft commutation inductor is produced by a  
10     phase shift full bridge topology depicted in Figure 8A.  
11     **Figure 13B** is a schematic diagram of an DC-DC Converter using the embodiment presented in Figure 4A,  
12     wherein the soft commutation inductor is split in two sections, one section transferred in primary section in series  
13     with the primary winding, and the other section in the secondary. The AC signal across the primary winding  
14     connected in series with one section of the soft commutation inductor is produced by a phase shift full bridge  
15     topology, depicted in Figure 8A. This structure being another embodiment of the invention.  
16     **Figure 13C** is a schematic diagram of an DC-DC Converter using the embodiment presented in Figure 4A,  
17     wherein the soft commutation inductor is transferred in primary section in series with the primary winding and  
18     providing a center tap, connected to a capacitor. The AC signal across the primary winding connected in series  
19     with one section of the soft commutation inductor is produced by a phase shift full bridge topology, depicted in  
20     Figure 8A. This structure being another embodiment of the invention.  
21     **Figure 13D** is a schematic diagram of an DC-DC Converter using the embodiment presented in Figure 4A,  
22     wherein the transformer is implemented by using two identical transformers connected in series. The additional  
23     circuit formed by an inductor in series with the capacitor is connected in between the primary ground and the  
24     connection between the two primary windings of the two transformers. The AC signal across the primary  
25     windings is produced by a phase shift full bridge topology, depicted in Figure 8A. This structure being another  
26     embodiment of the invention.

1      **Figure 14A** is a schematic diagram of an DC-DC Converter using the embodiment presented in Figure 4A, The  
2      AC signal across the primary winding of the transformer is produced by two phase shifted two transistor forward  
3      topologies. This structure being another embodiment of the invention.

4      **Figure 14B** is a timing diagram of the circuit of figure 14A.

5      **Figure 15** presents a magnetic-packaging structure suitable for the implementation of the embodiments of the  
6      invention.

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11     **Detailed Description of the Preferred Embodiments**

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13     For the AC-DC and DC-DC converters for high voltage application wherein the use of Schottky rectifiers is not  
14     possible due to high voltage across the rectifiers, one of the major obstacles is the reverse recovery loss of the  
15     rectifiers. The reverse recovery losses are proportional with the current slope through rectifier at turn OFF, the  
16     reverse voltage across the rectifier after the rectifier exhibits high impedance, the temperature, frequency of  
17     operation and the device characteristics. Additional snubber circuits are often used to reduce the voltage stress on  
18     the rectifiers during switching. The frequency of operation has to be also reduced which leads to poor volumetric  
19     efficiency of the converters. In Figure 2 are presented a prior art an AC-DC converter. An AC source drives the  
20     primary of the transformer T6, 950. There is inherent leakage inductance in the transformer, which acts as a  
21     current source during commutation of the rectifiers 406 and 408. In the right side of the rectifier there is another  
22     current source formed by 410. During switching transitions there are two unmatched current sources on both ends  
23     of the rectifiers. This leads to high voltage spikes across the rectifiers 406 and 498. Additional RC snubbers are  
24     necessary to maintain the voltage across the rectifiers below the breakdown voltage. This leads to higher power  
25     dissipation and high EMI.

26     In Figure 3A there is presented another prior art topology used for high voltage applications wherein an additional  
27     Lv, 12 , is added in the primary of the transformer Tr1. Additional clamping diodes D5 and D6 are also inserted.

1 The reverse recovery losses in the secondary rectifiers are reduced due to controlled current slope during  
2 switching. The limitation of the current slope is due to Lv. The presence of two-unmatched current source such as  
3 the Lv and 30 leads also to voltage spikes across the secondary rectifiers 22,28, 24 and 26. This requires snubbers  
4 circuits across the output rectifiers, which will reduce the efficiency of the converter.  
5 This invention proposes several circuits wherein there is not need for snubber circuits across the secondary  
6 rectifiers, and the reverse recovery losses are minimized and under certain conditions eliminated. The maximum  
7 voltage across the rectifiers in this invention is clamped to the output voltage. This will allow a very efficient  
8 operation at high frequency in high power and high voltage applications leading to an increase of the power  
9 density of the converter.  
10 In Figure 4A is depicted an AC voltage source Vs, 46. The voltage signal produced by 46 is presented on time  
11 diagram 60 in Figure 4B. From To to T1 the voltage source 46 provides a positive voltage, 154. The duration of  
12 this signal is referred as Ton. The Ton is the difference between T1and To. After T1 the voltage source 46,  
13 provides a zero amplitude voltage signal 156, exhibiting in the same time very low internal impedance. During the  
14 time interval T1-T2 , the voltage source 46 acts as a sort circuit. The current can flow bydirectional through 46,  
15 without developing a significant voltage drop. After T3, the voltage source 46, provides a voltage 158 of opposite  
16 polarity to 154 and the same amplitude. The time interval T3 to T4 when 46, provides 158, is equal to the time  
17 interval To to T1. The product of the time interval (T1-To) and the voltage amplitude 154 is equal to the product  
18 of the time (T4-T3) and the voltage amplitude of 158. After T4, the voltage source 46, is equivalent again to a  
19 short circuit providing a zero amplitude voltage. This state will apply for the time interval between T4 to T6. The  
20 time interval T1 to T3 and the time interval T4 to T6 are preferred to be equal, though it is not necessary. The  
21 embodiment of this invention will also apply if T3-T1 is not identical to T6-T4.  
22 This type of voltage source can be produced by a transformer and several controlled switchers as is depicted in  
23 figure 8A, 9Aand 14A. The method of control pictured in 8A is well known in the prior art.  
24 As is depicted in figure 4A in addition to the voltage source 46, there is an inductive element Lr, 48 and a bridge  
25 of rectifiers, 900, formed by rectifiers 50, 54, 52, and 56. The inductive element Lr is referred in this application  
26 as the soft commutation inductor element. The voltage source 46 is connected in series with inductor 48, and  
27 applied across the rectifier bridge 900 with one termination to the cathode of 56 and the anode of 50. The second

1 termination goes to the cathode of 52 and the anode of 54. A capacitor 58 is connected across the other two  
2 termination of the bridge, respectively between the anodes of 56 and 52 and the cathodes of 50 and 54. A load 902  
3 is connected across the capacitor 58.

4 During T0 to T1 when 46, produces a positive voltage 154 at the end connected to Lr, the current will flow through  
5 Lr, rectifier 50, rectifier 52 the capacitor 58 and the load 902. It is assumed that the voltage across 58 exhibits low  
6 voltage ripple much lower than the voltage amplitude produced by 46. With this assumption the current through  
7 Lr will build up linearly as pictured in 62 of Figure 4B, from zero to a peak value at T1. During this period of time  
8 the energy provided by 46, will be transferred to 902, and a part of energy will remain stored in Lr. During the  
9 time interval between T1 to T2 when the voltage source Vs is equivalent to a short circuit, the current through Lr  
10 will continue to flow until the entire energy stored in Lr will be transferred to the load 902. This will occur at T2,  
11 when the current through Lr will reach zero. During the interval T2 to T3 there is no energy transferred to the  
12 load. D01 and D01' ceases to conduct after the current through Lr reaches zero. A voltage ringing may occur  
13 across the rectifiers of bridge 900, as a result of the resonant circuit formed by Lr and the parasitic capacitance of  
14 the rectifiers, 50, 52, 54 and 56. The energy contained in this resonant circuit is very small, if the parasitic  
15 capacitance of the rectifiers is small. A saturable inductor element is in series with Lr may damp this oscillation if  
16 its energy content is too high. In the critical conduction mode of operation wherein the voltage produced by Vs  
17 will change polarity after the current through Lr reaches zero this ringing will not exist. The time interval between  
18 T2 and T3 can be controlled in such way that the polarity change of the voltage produced by 46 will occur after  
19 the ringing across the rectifiers forces the second set the rectifiers, which will conduct in the next cycle, in this  
20 case 56 and 54, in conduction. In this mode of operation there will be zero voltage switching for the rectifiers. The  
21 disadvantage of this mode of operation is the frequency modulation for load and line change. The advantage of  
22 this mode of operation is that we create ideal switching condition for the rectifiers. A combination of critical  
23 conduction through Lr and fix operating frequency for light load operation it may give the optimum operating  
24 mode. At the moment T3, the voltage source 46, changes its polarity and the current will start flowing linearly  
25 through Lr in the opposite direction. At the moment T4, when the voltage produced by 46, becomes zero, the  
26 current through Lr reaches its peak. Further between T4 to T5 the entire energy stored in Lr will be transferred to

1 the load 902. This will occur at the moment T5 when the current through Lr reaches zero. In between T5 and T6  
2 we have the same mode of operation as described between T2 and T3.  
3 The advantage of this mode of energy transfer from the source 46, to the load 902 is the fact that the voltage  
4 across all the rectifiers contained in the bridge 900 is clamped to the voltage across Co which is also the output  
5 voltage of the converter and the fact that the current through the rectifiers at turn OFF is zero. The voltage across  
6 all the rectifiers reverses only after the current reaches zero. This mode of operations eliminates reverse recovery  
7 losses, which is a significant advantage for high output voltage application. If the mode of operation is critical  
8 conduction through Lr, and the voltage commutation of 46, occurs after the current through Lr reaches zero and  
9 delayed by a time interval until the voltage across the rectifiers which will conduct at next cycle to reach zero, or  
10 its lowest level. The control of the voltage reversal of the voltage source 46 can be done through analogic circuits  
11 which sense the current through Lr and the voltage across the rectifiers, or can be done with microcontroller using  
12 digital signal processing.

13 In Figure 6A there is presented the same configuration as Figure 4A. The difference is the mode of operation,  
14 which is depicted in Figure 6B. After a positive voltage is applied by 46, and the current is built up through Lr,  
15 until the voltage source 46, becomes a short circuit. The current will continue to flow through Lr transferring its  
16 stored energy to the load. When the voltage produced by Vs changes its polarity there is current present through  
17 the Lr. The voltage across Lr is the sum between the output voltage 904 and the voltage across Vs, 158. The  
18 current through Lr will decrease at a higher rate and will reach zero at T8. Between T3 and T8 the current will  
19 force the rectifier 50 and 52 to continue to conduct. The reverse of conduction will occur at T8, when the rectifier  
20 56 and 54 will be forced into conduction. In this mode of operation there are reverse recovery losses due to the  
21 conduction of the rectifiers when the reverse voltage is applied to them. The reverse recovery losses are not high  
22 due to the fact that the rate of current change through rectifiers at turn off is limited by Lr. In addition to that the  
23 reverse voltage across the rectifiers is clamped to the output voltage 904. During the time interval T3 and T8 and  
24 T6 to T9, the energy is transferred from the Lr to the voltage source. In conclusion during T7 to T1 and  
25 respectively T8 and T4 the energy is transferred from the primary to the load and to the Lr. During the time  
26 interval T0 to T7 and respectively T3 and T8, the energy is transferred from Lr to the source. This kind of  
27 operation is less efficient than the one presented in Figure 4A. In most of applications this mode of operation

1 referred as continuous conduction mode can occur during the transient situations. The current through the Lr is  
2 depicted in 162. The voltage across the rectifiers is depicted in 164 and 168. The current through 50 and 52 is  
3 depicted in 166. In 170 is depicted the current through 56 and 54.

4 It is very important to underline the fact that the key advantage of this invention is the energy transferred from  
5 primary to secondary is done in one direction only, if the operation occurs in discontinuous mode. The voltage  
6 source Vs would not exhibit short circuit characteristics during T1 to T3 and T4 to T5, the energy will be also  
7 transferred from the load to the primary. This limits the numbers of topologies, which can be used in the primary  
8 side, capable to provide the right characteristics for Vs.

9 In the circuit presented in Figure 5A and 6A the energy transferred from the Vs to the load is function of the  
10 voltage across Vs, the output voltage 904 and the inductor Lr. The circuit 7A presents a method of power  
11 transferred wherein the amount of energy transfer for a given Vs, Lr and Vo can be further increased and  
12 modulated by the additional bydirectional switch S2. The additional switch S2 does not have to be bydirectional.  
13 The bydirectional switch will maintain the symmetry of the energy transfer for the positive cycle 154 and negative  
14 cycle 158. A unidirectional switch will modulate the power only for positive or negative cycle. The timing  
15 diagram on Figure 7B is referring to a bydirectional switch. The control signal for the switch S2, 336, is  
16 synchronized with the voltage source Vs. The switch is turned ON when a positive polarity voltage 154, and a  
17 negative polarity voltage 158 is ramping up from Vs. During the time interval from To to T10, a positive voltage  
18 154 is provided by Vs, and the switch 336 is ON. As a result the current will flow through Lr with a slope  
19 determined by the amplitude of 154 and the value of Lr. The value of the output voltage 904 does not play any  
20 role. The current slope in between To and T10 is high and more energy is stored to Lr during this interval. When  
21 the switch S2 is turned OFF at the moment T10 the current which flows through Lr will turn ON the rectifiers 50  
22 and 52, transferring the energy to the load 902. The current continues to build up through Lr at a smaller rate  
23 imposed by the difference between the amplitude of 154 and the output voltage. At the moment T1 the current  
24 through Lr reaches its peak. From T1 to T2 all the energy contained in Lr will be transferred to the output if the  
25 unit operates in discontinuous mode, as is depicted in Figure 7B. The unit can also operate in continuous mode,  
26 wherein the current will not reach zero before the voltage Vs will reverse its polarity. When the voltage Vs  
27 changes its polarity at T3, the switch S2 will be also turned on and the current will build up through Lr with the

1 same slope as between To to T10, but of opposite polarity. The major advantage of this embodiment over the  
2 embodiment presented in Figure 4A and 6A, is the fact that the energy transfer from Vs to Lr is independent of Vo  
3 during the To to T10, respectively T3 to T12 period. The energy transferred during a given time is higher without  
4 increasing the amplitude of 154. The output power can be also modulated not only by the ratio of the ON time  
5 which is the summation of the (T1-To) and (T4-T3) and the period of the signal depicted in 160. The output  
6 power can be further modulated by the ON time of S2.

7 Figure 10A is an extension of the embodiment depicted in Figure 4A wherein the rectifiers 56 and 52 are replaced  
8 by the controlled synchronized rectifiers M10, 802, and M11, 804. These synchronous rectifiers are controlled by  
9 the Vc2 and Vc1 depicted in 700 and 702. The use of synchronous rectifiers may have the advantage of lower  
10 voltage drop, which translates in a higher efficiency. Between To to T1 when a positive voltage 154 is applied to  
11 Lr, the current will flow through D01 and M11. The control signal 908 turns ON the M11 at To. The control  
12 signal 908 has to keep M11, turned ON until T2. The control signal Vc1 can be maintain high even after T2  
13 without impacting the mode of operation. This is a major advantage for using synchronous rectifiers because the  
14 timing at turn OFF is not very critical. Important is to turn OFF, Vc1 prior the T3.

15 Another embodiment of this invention is presented in figure 11A. The bridge 900 is formed by the synchronous  
16 rectifiers controlled by controlled signals Vc1 and Vc2. The timing diagram for Vc1 and Vc2 are depicted in  
17 figure 11B in 704 and 706. The mode of operation for the converter depicted in Figure 11A is the same as the one  
18 depicted in Figure 4A for discontinuous and critical conduction mode and the one depicted on 6A for the  
19 continuous conduction mode.

20 Another embodiment of the invention is presented in Figure 5A. The circuit formed by the voltage source Vs and  
21 the Lr in series is connected to a bridge formed by two rectifiers 134 and 136 and two capacitors 138 and 140. The  
22 output voltage 904 is the voltage across the two capacitors 138 and 140. The output voltage is further applied to a  
23 load. In this there are used only two rectifiers. Between To and T1 the voltage source Vs provides a positive  
24 polarity voltage 154 at the end connected to Lr. The current will flow through Lr , D01 and C01. At T1 the current  
25 through Lr reaches its peak. Between T1 to T3 the source 46 becomes a short circuit 156. The current continuos to  
26 flow through Lr until reaches zero at T2. At that time all the energy stored in Lr is transferred to the C01 and  
27 Load, via Vo. At T3 the voltage polarity produced by 46 reverses. The current will flow from the voltage source

1 Vs through Co2, Do2 and through Lr in an opposite direction to the flow in the previous cycle. The load is applied  
2 across the series combination formed by Co1 and Co2. This circuit maintains the same advantages of the circuit  
3 depicted in Figure 4A. The voltage across each rectifier is clamped to the output voltage. The current through  
4 rectifiers reaches zero prior to the application of a reverse voltage across them. As a result the reverse recovery  
5 losses are eliminated. If the converter operates in critical conduction mode, wherein the voltage polarity of 46  
6 changes after the current through 48 reaches zero, with a delay necessary for the voltage across the rectifier which  
7 will conduct at next cycle reaches zero or close to zero, we can reach zero voltage or near zero voltage  
8 commutation for the rectifiers. The circuit depicted in Figure 5A can also operate in continuous conduction mode  
9 as the circuit depicted in Figure 6A. In Figure 12A the rectifiers 134 and 136 are replaced by two controlled  
10 synchronous rectifiers 810 and 812. The control signals Vc1 and Vc2 are depicted in Figure 12B in 708 and 710.  
  
11 In order to produce the Vs in the secondary of a transformer there are presented three circuits, which are suitable  
12 to produce such a source. One of these circuits is presented in Figure 8A. The timing diagram associated with this  
13 circuit is presented in Figure 8B. This circuit is familiar to those skilled in the art. It is known as phase shift full  
14 bridge. It is formed by two complementary half bridges, one formed by M1 and M2 and another one formed by  
15 M3 and M4. The control signals for M1 and M4 are presented in 80. The controlled signals for M3 and M4 are  
16 presented in 82. During the conduction of M1 and M4 the input voltage is applied to the primary winding 110 of  
17 the transformer T2. The voltage induced in the secondary winding 112 is positive in reference to the arrow 116. In  
18 the secondary winding 112 there will be a voltage referred previously as 154. When the M4 turns OFF the current  
19 will continue to flow through the primary winding 110, and further through the body diode of M3 , creating zero  
20 voltage switching condition for M3 which is turned on at zero voltage. During the time when M1 and M3 conduct,  
21 the primary winding of 106 is shorted. In the secondary, the Vs will be zero and a short-circuit characteristics.  
22 This is equivalent to what previously was referred as 156. At the moment when M1 turns OFF the current will  
23 continue to flow through 110 and the drain to source capacitance of M2 creating zero voltage or near zero voltage  
24 conditions for M2. The voltage applied to primary winding 110 will change the polarity applying a negative  
25 voltage in reference to the arrow 112. This is equivalent to what previously was referred as 158. When M3 is  
26 turned OFF the current continue to flow through 110 discharging the drain to source capacitance of M4 to zero or

1 near zero, creating zero or near zero voltage switching conditions for M4. When M2 and M4 conduct the primary  
2 winding 110 is shorted and in the secondary the state of Vs is as short circuit 156.

3 The circuit presented in Figure 8A , which is known as phase shifted full bridge converter can generate in the  
4 secondary of the transformer the voltage source used in describing our embodiments. What differentiate the circuit  
5 of Figure 8A from other circuits which can generate a voltage source, is the short circuit behavior 156 during the  
6 time when the voltage in secondary is zero.

7 The combinations of the circuits presented in Figure 4A, 6A, 7A 5A, 10A, 11A and 12A with the full bridge phase  
8 shifted topology depicted in 8A, has another advantage. The slow rising the current through Lr in the secondary  
9 will allow the full swing towards zero voltage across all the switchers in the primary. A fast current ramp in the  
10 secondary winding which is specific to the prior art topologies as depicted in 2 and 3A the soft switching in the  
11 primary is difficult to achieve for one of the complementary half bridge. This is due to the fact that the fast rise of  
12 the current in the secondary will steal some of the primary current flowing through the resonant tank formed by  
13 the magnetizing inductance of the transformer and the parasitic capacitance of the switchers.

14 Another circuit capable to provide the secondary voltage Vs with the bydirectional low impedance characteristics  
15 during 156, is depicted in figure 9A. This topology is not known by those skilled in the art. This topology is a  
16 modification of a conventional half bridge converter with the addition of a supplementary bydirectional auxiliary  
17 switch S1. The timing diagram is depicted in Figure 9B. The switching elements 118 and 120 are controlled by the  
18 signals 122 and 124. The control signals 122 and 124 have the same duration, in between these two signals is a  
19 dead time. By increasing the duration of 122 and 124 and accordingly decreasing the duration of the dead time,  
20 the power transferred to the output can be controlled. An additional control signal 132 controls the bydirectional  
21 switch S1. The control signal 132 is turning the switch 334 ON during the dead time 910. There is a dead time  
22 between the falling edge of 122 and the rising edge of 132. There is also a dead time between the falling edge of  
23 132 and rising edge of 124. This delay time is necessary to allow the voltage across the switching elements 118 ,  
24 120 and 334 to swing in order to achieve zero voltage-switching conditions. In Figure 9B as is depicted on 88, the  
25 voltage across the switching element 120, VM2, has a soft transition from Vin level to a voltage plateau Vin/2  
26 during the conduction of S1 and further a soft commutation to zero after the falling edge of 132. The current  
27 through switching element 120 is depicted on 90. During the conduction of 118 there is a voltage in the secondary

1 winding 112 of the transformer T2. This is equivalent to 154. During the conduction of 120 there is a negative  
2 voltage across 112 , equivalent to 158. During the conduction of 132, there is a short circuit across the primary  
3 winding 110, which reflects in the secondary winding 112. This state is equivalent to 156.

4 The topology described in Figure 9A provides in the secondary winding 112 of the transformer 106 the voltage  
5 source with the characteristics required in our embodiments. In addition to this, the circuit of Figure 9A offers  
6 zero voltage switching conditions for both switching elements, and recycles the leakage inductance energy which  
7 is not dissipate, but used for discharging the parasitic capacitance of 118, 120 and 334.

8 A third circuit capable to produce the required voltage source characteristics of Vs, is presented in Figure 14A.  
9 There are two power trains, formed by two transistor forward topologies. The first power train contains two

10 switching elements M11 and M12, controlled by the same control signal Vc11, 968. The first power train contains  
11 also a transformer T11, 988. The second power train contains two switching elements M13 and M14. Both

12 switching elements are controlled by the same control signal, Vc13, 972. In the second power train there is a  
13 transformer T12, 990, which has the secondary winding 980 in series with the secondary winding 978 of the  
14 transformer 988. The timing for Vc11 and Vc13 is presented in Figure 14B, on 992 and 994. The power is  
15 modulating by the phase shift between the Vc11 and Vc13. The voltage in the secondary of the transformers 988  
16 and 990 will subtract during the overlapping time of Vc11 and Vc13, creating in the secondary the 156 signal.

17 In the secondary in series with the secondary windings 978 and 980, there is the soft commutation inductive  
18 element Lr. The secondary rectifier means and the output filter is the one described in Figure 4A.

19 In Figure 1A is depicted a circuit wherein the embodiment of claim 4A is combined with the circuit described in  
20 Figure 8A. There is an additional circuit formed by an inductor element 440 and a capacitor 442, The additional  
21 circuit creates a triangular current waveform which is superimposed on the currents through M1 and M2. In Figure  
22 1B is presented the timing diagrams of the key waveforms of the circuit illustrated in Figure 1A. The control  
23 signals for M1 and M2 are presented on 914. The control signal for M3 and M4 is presented on 916. The  
24 triangular shaped additional current 922 flowing through 440 and 442 are presented on 918. The current 924  
25 flowing through M1 is the result of the superposition of the 922 and the current reflected from the secondary of  
26 the transformer. The presence of 918 allows zero voltage switching conditions for M1 and M2. The additional  
27 current 922 will add to the magnetizing current of transformer T2 and discharge the parasitic capacitance of M1

1 and M2 prior the switchers M1 and M2 are turned ON. The magnitude of 922 is controlled by the size of 440. A  
2 lower inductance of 440 will increase the additional current 922 . This will ensure the zero voltage switching  
3 conditions for M1 and M2. The switchers M3 and M4 have an inherent zero voltage switching characteristics. If  
4 zero voltage switching has to be reached even at zero phase shift on both section of the full bridge, a similar  
5 circuit formed of an inductor in series with a capacitor can be inserted between the GND and the M3 and M4 at  
6 the node where the transformer T2 is inserted. The voltage across the 442 and the additional capacitor is the same  
7 and equal to Vin/2. As a result the circuit can be simplified by connecting only one inductor with center tap across  
8 the primary winding 110. The center tap of the additional inductor can be further connected to a capacitor which  
9 has the second termination connected to the GND. The capacitor 442 can be also formed by two capacitors in  
10 series one connected to the positive end of the Vin and the second capacitor connected to the negative end of 130.

11 The common node of these capacitors is connected to 440. In figure 13A is presented the combination of the  
12 circuit presented in Figure 4A and the full bridge phase shifted circuit depicted in Figure 8A. The circuit presents  
13 another embodiment of the invention wherein the inductor element Lr 48 is transferred in the primary of the  
14 transformer T2. The mode of operation is similar with the circuit wherein the inductor element Lr is located in the  
15 secondary of the transformer. One advantage of this circuit is the fact that the current flowing through Lr will help  
16 to achieve zero voltage switching conditions for the primary switchers 92, 96, 94 and 160, with the penalty of an  
17 increase in the flux density in the transformer's core 108.

18 In figure 13B the soft commutation inductor is split in two elements, one in the primary of the transformer 48A  
19 and one in the secondary of the transformer 48B. The ratio between 48B and 48A reflected in the secondary can  
20 be chosen for the optimization of the circuit. The optimization will be chosen for different criteria function of the  
21 priority of the design. It is important to understand that Lr, Lr1 or Lr2 can be implemented by the leakage  
22 inductance of the transformer. An additional discrete inductive element in series with the equivalent leakage  
23 inductance may or may not be necessary, function of the application.

24 In Figure 13C the soft commutation inductor element is split in two section 48C and 48D. These two sections are  
25 implemented on the same magnetic core 930. An additional capacitor Czvs 932 is inserted in between the 48C and  
26 48D and the ground. The same effect can be reached if the 932 will be connected to positive end of 130.

1 There are two transformers T2 and T600, which have the primary windings 110 and 606 in series and the  
2 secondary windings 620 and 608 also in series. The invention does not limit to two transformers. It can be a  
3 number of transformers, preferable an even number and the connection to the capacitor 932 will be done in the  
4 middle having an equal number of transformers at each side of the connection.

5 This circuit formed by 932, 48C and 48D will add supplementary currents, which will assist in achieving, zero  
6 voltage switching for 92, 96 , 94 and 160. When the diagonal switchers are conducting such as 94 and 96 or 92  
7 and 160, the combination LrC and LrD will exhibit a higher impedance calculated in a such way to achieve  
8 optimum energy transferred to the secondary as presented in Figure 13A. When the upper switchers 92 and 94 or  
9 the lower switchers 96 and 104 conduct the impedance between the end of 932 not connected to the GND, and the  
10 transformers T2 and T600 primary winding is very small. This will lead to circulating currents through 932, which  
11 will allow zero voltage switching conditions even at zero phase shift. This is very important in applications

12 wherein zero voltage switching can be accomplished regardless of the phase shift.

13 *depicts*  
14 In figure 13D is depicted a circuit wherein the soft commutation inductor 48, is transferred to the secondary, and  
15 the LrC and LrD is substituted by Lzv 440. The combination 440 and 442 is connected in between the T2 and  
16 T600. This circuit has the advantage of providing an additional triangular current through both sections of the full  
17 bridge, M1 and M2 and also M3 and M4. This structure can offer zero voltage switching conditions on all four  
18 switching elements, 92, 96, 94 and 160 regardless of the phase shift, even at zero phase shift. This circuit offer  
19 significant advantages over the prior art, such as soft switching across the rectifiers 50, 52, 54 and 56, and also  
across all the switching elements in the primary regardless of load, input voltage and phase shift.

20 Many alterations and modifications may be made by those having ordinary skill in the art without departing from  
21 the spirit of the invention. For example, is the use of several transformers on each side of the connection between  
22 440, 616, and 606. The capacitor 442 can be implemented by using two capacitors in series which have the non-  
23 common node connected to each end of Vin, 130.

24 *presents*  
25 In Figure 15 is presented a packaging concept suitable with this invention. All the switching elements such as  
26 200a, 200b, 200c ,200d and 214a, 214b, 214c and 214d, are attached on a multilayers board 202, and cooled by  
means of via or thermally conductive inserts located under the switching elements to a base plate 932 attached  
27 under the multilayers boards 202. In between the base plate 932 and multilayers board 202 there is a thermally

1 conductive insulation material 934. The magnetic elements are constructed using spiral traces inside of the  
2 multilayer board 202 with cutouts 218, to allow the magnetic cores 216 to penetrate through and to close the  
3 magnetic circuit with second magnetic core 936 attached from the bottom of the 202. The thermally conductive  
4 plate is interrupted under the magnetic core or it can provide cavities to accommodate them. A supplementary soft  
5 elastic material 938 with good thermal conductivity is inserted in between the core and the metal plate. Some  
6 additional electronic components such as 210, 208 can also be placed on 202. Pressed connectors such as 204a,  
7 204b, 206b and 206c can be inserted in 202 to offer a low impedance path for the input and the output current to  
8 an external mother PCB. The advantage of this packaging is the reduction of the stray impedance associated with  
9 the interconnection between the switching elements and the magnetic elements. It offers also a solid mechanical  
10 construction suitable for demanding working environment conditions.

11 The invention is defined by the following claims wherein may be substituted therein for obtaining substantially the  
12 same result even when not obtained by performing substantially the same function in substantially the same way.  
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